LZ95G55

Single-Chip Driver LSI for CCD

DESCRIPTION

The LZ95G55 is a CMOS single chip driver LSI which provides timing pulses used to drive a CCD area sensor, and generates synchronous pulses for TV signals and processing pulses for video signals.

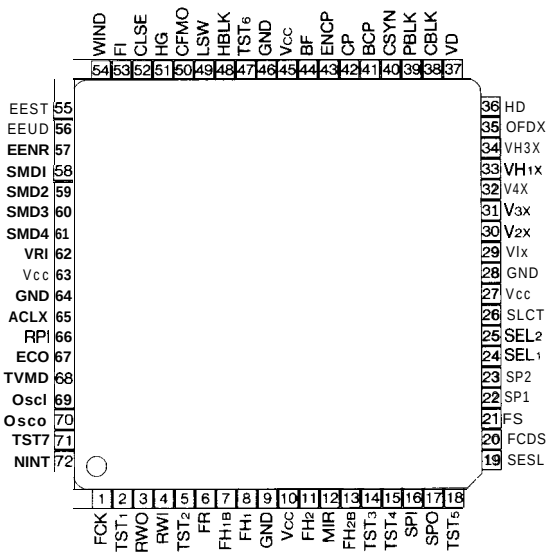
FEATURES

- Switchable between 270000 pixels CCD and 320000 pixels CCD
- Switchable between NTSC (EIA) and PAL (CCIR) systems
- Built-in EE (Electronic Exposure) control (1/60 to 1/100 000 s for NTSC; 1/50 to 1/100 000 s for PAL)
- Internal electronic shutter : Shutter speed is selectable from 1/60 (PAL : 1 /50), 1 /250, 1 /500, 1/1 000, 1/2 000, 1/4 000 and 1/10 000 s, in addition to this, plus 1/100 s(PAL : 1/120 s) in Flicker-less mode using parallel code
- Switchable between Electronic Shutter mode and EE Control mode
- Switchable between normal and mirror image
- No-interlace mode is possible
- External synchronization is possible
- Included phase comparator circuit
- Single +5 V power supply

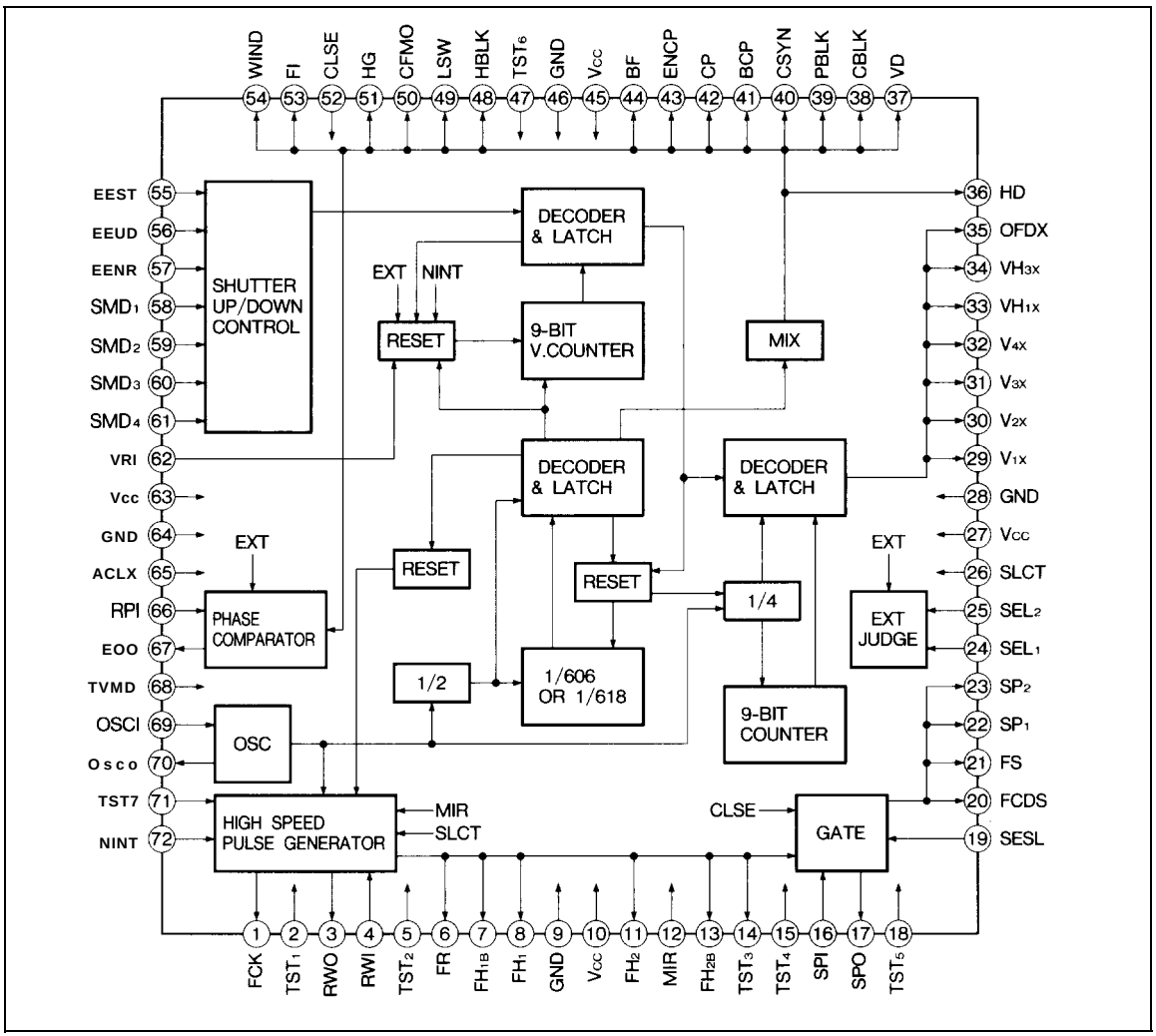
. Package : 72-pin QFP(QFP072-P-101 O)

PIN CONNECTIONS

72-PIN QFP — TOP VIEW



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to + 7.0	V
Input voltage	V_I	−0.3 to V_{CC} + 0.3	V
Output voltage	V_O	−0.3 to V_{CC} + 0.3	V
Operation temperature	Topr	−20 to +70	°C
Storage temperature	Tstg	−55 to +150	°C

DC CHARACTERISTICS

(V_{CC} = +5 V* 10%, Ta = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1.5	V	1
Input High voltage	V_{IH}		3.5			V	
Input Low voltage	V_{T+}				3.7	V	2
Input High voltage	V_{T-}		1.0			V	
Hysteresis voltage	$V_{T+} - V_{T-}$		0.4			V	
Input Low current	$\lvert I_{IL1} \rvert$	V_I = 0 V			1.0	μA	3
	$\lvert I_{IL2} \rvert$	V_I = 0 V	8.0		60	μA	4
Input High current	$\lvert I_{IH1} \rvert$	$V_I = V_{CC}$			1.0	μA	5
	$\lvert I_{IH2} \rvert$	$V_I = V_{CC}$	8.0		60	μA	6
Output High voltage	V_{OH1}	I_{OH} = −2 mA	4.0			V	7
Output Low voltage	V_{OL1}	I_{OL} = 4 mA			0.4	V	
Output High voltage	V_{OH2}	I_{OH} = −3 mA	4.0			V	8
Output Low voltage	V_{OL2}	I_{OL} = 4 mA			0.4	V	
Output High voltage	V_{OH3}	I_{OH} = −6 mA	4.0			V	9
Output Low voltage	V_{OL3}	I_{OL} = 8 mA			0.4	V	
Output High voltage	V_{OH4}	I_{OH} = −9 mA	4.0			V	10
Output Low voltage	V_{OL4}	I_{OL} = 12 mA			0.4	V	
Output High voltage	V_{OH5}	I_{OH} = −9 mA	4.0			V	11
Output Low voltage	V_{OL5}	I_{OL} = 18 mA			0.4	V	
Output High voltage	V_{OH6}	I_{OH} = −6 mA	4.0			V	12
Output Low voltage	V_{OL6}	I_{OL} = 12 mA			0.4	V	
Leak output current	$\lvert I_{OZ} \rvert$	High-Z			1,0	μA	

NOTES :

1. **Applied to inputs (IC,** ICD, ICU).
2. **Applied to inputs** (ICSU).
3. **Applied to inputs** (IC, ICD).
4. Applied to inputs (ICU, ICSU).
5. Applied to inputs (IC, ICU, ICSU).
6. Applied to input (ICD).
7. Applied to outputs (O, ORI, OSC).
   {Output (OSC) measures on conditions that input (IBF0) level is O V or V_{CC}.)
8. Applied to output (ORA).
9. Applied to output (ORB).
10. Applied to output (ORC).
11. Applied to output (ORD).
12. Applied to tri-state output (TO).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	FCK	OR1		Clock output for delay line	A pulse for clock of CCD delay line, The frequency of the signal is 1/2 the frequency of the OSCI.
2	TSTI	ICD	–	Test terminal 1	A test pin. Set open or to L level in the Normal mode.
3	RWO	oRA		Width of FR control output	A pulse to control pulse width of FR (pin 6). Connect to RWI (pin 4) pin through CR delay circuit,
4	RWI	IC	–	Width of FR control input	An input pin to control pulse width of FR. Trailing edge of FR is defined by rising edge of input pulse.
5	TST2	ICD	–	Test terminal 2	A test pin. Set open or to L level in the Normal mode.
6	FR	ORC		Reset pulse	A reset pulse for CCD, Connect to ϕ_R of CCD through the DC offset circuit.
7	FH_{IB}	ORB		Horizontal transfer pulse 1 B	A horizontal transfer pulse for mirror CCD. Connect to ϕ_{H1B} of CCD.
8	FH,	ORD		Horizontal transfer pulse 1	A horizontal transfer pulse for CCD. Connect to ϕ_{HI} of CCD.
9	GND	–	–	Ground	A grounding pin.
10	Vcc	–	–	Power supply	Supply +5 V power.
11	FH2	ORD		Horizontal transfer pulse 2	A horizontal transfer pulse for CCD. Connect to ϕ_{H2} of CCD.
12	MIR	ICU	–	Mirror mode select	An input pin to select Mirror mode or Normal mode. L level : Normal Drive mode H level or open : Mirror Drive mode
13	FH_{2B}	ORB		Horizontal transfer pulse 2B	A horizontal transfer pulse for mirror CCD. Connect to ϕ_{H2B} of CCD.
14	TST3	ICD	–	Test terminal 3	A test pin. Set open or to L level in the Normal mode.
15	TST4	ICD	–	Test terminal 4	
16	SPI	IC	–	Timing of SP_1, SP2 control input	An input pin to control pulse timing of SPI, SP2.
17	SPO	ORA		Timing of SP_1, SP2 control output	A pulse to control pulse timing of SP_1, SP_2. Connect to SPI (pin 16) pin through the CR delay circuit.
18	TST5	ICD	–	Test terminal 5	A test pin. Set open or to L level in the Normal mode.
19	SESL	Icu	–	SPO control input	An input pin to switch phase of SPO. H level or open : The pulse is delayed by 52 ns from RWO. L level : The pulse is nearly RWO pulse.
20	FCDS	ORB	n	CDS pulse 1	A pulse to clamp the feed-through level from CCD.
21	FS	ORB		CDS pulse 2	A pulse to sample-hold the signal from CCD.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>I/O</th><th>POLARITY</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>22</td><td>SP1</td><td>ORB</td><td>n</td><td>Color sampling pulse 1</td><td>A pulse to output the sampling for color demodulation based upon the output signal of CCD.</td></tr>
<tr><td>23</td><td>SP2</td><td>ORB</td><td>⎍</td><td>Color sampling pulse 2</td><td>A pulse to output the sampling for color demodulation based upon the output signal of CCD.</td></tr>
<tr><td>24</td><td>SELI</td><td>ICU</td><td>–</td><td>External Synchronization mode select 1</td><td rowspan="2">Select External Synchronization mode.
<table><tr><th>SEL1</th><th>SEL2</th><th>Mode description</th></tr><tr><td>L</td><td>L</td><td>Internal Synchronization mode</td></tr><tr><td>H</td><td>L</td><td>External Synchronization mode 1
: VD or line
RPI input
: external VD (negative) or line</td></tr><tr><td>L</td><td>H</td><td>External Synchronization mode 2
: Composite Synchronization mode
VRI input : VSYNC (negative)
RPI input : CSYNC (negative)</td></tr><tr><td>H</td><td>H</td><td>External Synchronization mode 3
: HD and VD Synchronization
VRI input : external VD (negative)
RPI input : external HD (negative)</td></tr></table></td></tr>
<tr><td>25</td><td>SEL2</td><td>ICU</td><td>–</td><td>External Synchronization mode select 2</td></tr>
<tr><td>26</td><td>SLCT</td><td>ICU</td><td>–</td><td>CCD select input</td><td>An input pin to select sensor type.
<table><tr><td>SLCT</td><td>L</td><td>H or open</td></tr><tr><td>CCD</td><td>Type A</td><td>Type B</td></tr></table>Type A : LZ2313A9/LZ2323A9, LZ23132/LZ23232
Type B : IZ2313B5/LZ2323B5, LZ2313H5/LZ2323H5</td></tr>
<tr><td>27</td><td>Vcc</td><td>–</td><td>–</td><td>Power supply</td><td>Supply +5 V power.</td></tr>
<tr><td>28</td><td>GND</td><td>–</td><td>–</td><td>Ground</td><td>A grounding pin,</td></tr>
<tr><td>29</td><td>V1X</td><td>o</td><td>⎍</td><td>Vertical transfer pulse 1</td><td>A vertical transfer pulse for CCD. To be connected to the 1 AX pin of vertical driver LSI.</td></tr>
<tr><td>30</td><td>V2X</td><td>o</td><td>⎍</td><td>Vertical transfer pulse 2</td><td>A vertical transfer pulse for CCD. To be connected to the 2AX pin of vertical driver LSI.</td></tr>
<tr><td>31</td><td>V3X</td><td>o</td><td>⎍</td><td>Vertical transfer pulse 3</td><td>A vertical transfer pulse for CCD. To be connected to the 3AX pin of vertical driver LSI.</td></tr>
<tr><td>32</td><td>V4X</td><td>o</td><td>⎍</td><td>Vertical transfer pulse 4</td><td>A vertical transfer pulse for CCD. To be connected to the 4AX pin of vertical driver LSI.</td></tr>
<tr><td>33</td><td>VH1X</td><td>o</td><td>⎍</td><td>Read out pulse</td><td>A pulse that transfers the charge of the photodiode to the vertical shift register.
Connected to the 1 BX pin of the vertical driver LSI.</td></tr>
<tr><td>34</td><td>VH3X</td><td>o</td><td>⎍</td><td>Read out pulse</td><td>A pulse that transfers the charge of the photodiode to the vertical shift register.
Connected to the 3BX pin of the vertical driver LSI.</td></tr>
<tr><td>35</td><td>OFDX</td><td>o</td><td>u</td><td>OFD pulse output</td><td>A pulse that sweeps the charge of the photodiode for electrical shutter. Connect to OFD of CCD through the invert, level shift and DC offset circuit. It is held at H level in Normal mode,</td></tr>
</table>

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
36	HD	o		Horizontal drive pulse	The pulse occurs at the start of lines.
37	VD	o		Vertical drive pulse	The pulse recurs at the start of every field,
38	CBLK	o		Composite blanking pulse	Composite blanking pulse.
39	PBLK	o		Pre-blanking pulse	Equivalent to CBLK (pin 8) pulse except for shorter pulse width with cut-off falling edge.
40	CSYN	o		Composite synchronizing pulse	Composite synchronous signal output pin.
41	BCP	o		Optical black clamp pulse	A pulse to clamp the optical black signal. This pulse stays low during the absence of effective pixels within the vertical blanking.
42	CP	o		Clamp pulse	CP is the same as BCP (pin 41) except that CP is delayed by 700 ns from BCP.
43	ENCP	o	n	Encoder DC clamp pulse	A clamp pulse that is used for recovering DC level. The repetition is horizontal frequency.
44	BF	o		Burst flag	A pulse to define burst period.
45	Vcc	–	–	Power supply	Supply +5 V power.
46	GND	–	–	Ground	A grounding pin.
47	TST6	ICD	–	Test terminal 6	A teat pin. Sat open or to L level in the Normal mode.
48	HBLK	o		Horizontal blanking pulse	A pulse that corresponded to the cease period of the horizontal transfer pulse.
49	LSW	o		Line switch	The signal switches between H and L at every line in PAL mode. It is set at Low level at the 1st line of the 1st field.
50	CFMO	o		Color frame output	A pulse to control color frame. Occurs at every 4 fields in NTSC mode. Occurs at every 8 fields in PAL mode.
51	HG	o		Line index pulse	The pulse is used in color separator. The signal switches between H and L at every line. Its reset point is changed by SLCT (pin 26). For details, see “NOTE 1”.
52	CLSE	ICD	–	Color sampling pulse control input	An input pin to control SPI, SP2 pulse correspond to color separator in signal processor.

CLSE input	Output to sample hold at color separator.
L level or open	SPI : Output contain Ye signal. SP2 : Output contain Cy signal.
HG pulse	SP1 : Output contain Mg signal. SP2 : Output contain G signal.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
53	FI	o	⊓	Field index	The pulse is used for detecting field. At NTSC mode : ODD field; LOW EVEN field; HIGH At PAL mode : 1st and 3rd fields; LOW 2nd and 4th fields; HIGH
54	WIND	o	u	Wind pulse	A pulse for wind pulse. When connected to EEST (Pin 55), the operation of Electronic Exposure can be stopped at the upper side of monitor.
55	EEST	ICU	–	Electronic Exposure control 1	An input pin to control Electronic Exposure, with using EEUD (pin 56) and EENR (pin 57). L level : Electronic Exposure is stopped. H level or open : Electronic Exposure is operated.
56	EEUD	IC	–	Electronic Exposure control 2	Input pins to control Electronic Exposure.
57	EENR	IC	–	Electronic Exposure control 3	
58	SMDI	Icu	–	Shutter control 1	Input pins to set up fixed shutter speed or to control Electronic Exposure mode. For details, see "NOTES 2, 3"
59	SMD2	Icu	–	Shutter control 2	
60	SMD3	ICU	–	Shutter control 3	
61	SMD4	ICU	–	Shutter control 4	
62	VRI	ICSU	–	Vertical reset input	An input pin for resetting internal Vertical counter. For inputs of SELI (pin 24) and SEL2 (pin 25), input pulse and the point of resetting is changed.
63	Vcc	–	–	Power supply	Supply +5 V power.
64	GND	–	–	Ground	A grounding pin.
65	ALCX	Icu	–	All clear input	An input pin for resetting all internal circuit at power on.
66	RPI	Icu	–	Horizontal comparison input	An input pin for the reference signal to the phase comparator, at External Synchronization mode. For inputs SELI (pin 24) and SEL2 (pin 25), input pulse is changed.

EEUD	EENR	Shutter speed control
H	L	up
H	H	stop
L	H	down

SEL_1	SEL_2	VRI input
X	L	–
L	H	External VSYNC (negative)
H	H	External VD (negative)

SELI	SEL2	RPI input
L	L	–
H	L	External VD (negative) or line
L	H	External CSYNC (negative)
H	H	External HD (negative)

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
67	EOO	TO	–	Phase comparator output	**At External Synchronization mode, phase comparator output for input signal RPI (pin 66) and internal comparison signal.** **When RPI is advanced, output is High level.** **When RPI is delayed, output is Low level.** **When phases are equal, the terminal impedance is High.**
68	TVMD	ICU	–	**TV mode select**	**An input pin to select TV standards.** **L level : NTSC, EIA mode** **H level or open : PAL, CCIR mode**
69	OSCI	IBF0	–	Clock input	**An input pin for reference clock oscillation.** **The frequencies are as follows :** **At NTSC mode : 1212 fH** **At PAL mode : 1236 fH** **(fH = Horizontal frequency)**
70	**Osco**	**Osc**	–	**Clock** output	**An output pin for reference clock oscillation.** The output is the inverse OSCI (pin 69).
71	TST7	ICD	–	Test terminal 7	A teat pin. Set open or to L level in the Normal mode.
72	NINT	ICD	–	Non-interlace select	An input pin to select Non-interlace mode. L level or open : Interlace mode H level : Non-interlace mode

IC : Input pin (CMOS level)
ICU : Input pin (CMOS level with pull-up resistor).
Icsu : Input pin (CMOS schmitt-triger level with pull-up resistor)
ICD : Input pin (CMOS level with pull-down resistor).
O, OR1 , ORA, ORB, ORC, ORD : Output pin.
TO : Output pin (tri-state output).
IBF0 : Input pin for oscillation.
Osc : Output pin for oscillation.

NOTE :

1. Timing of HG **(Line index pulse)**

MIR (pin 12)	X	X	X	X
SLCT (pin 26)	L	L	H	H
TVMD (pin 68)	L	H	L	H
Reset line	11 H	7 H	273 H	319 H
Reset level	L	L	H	H

2. Fixed Shutter mode

SMD1 (Pin 58)= Low level

SMD2 (Pin 59)	SMD3 (Pin 60)	SMD4 (Pin 61)	SHUTTER SPEED (s) NTSC	PAL
L	L	L	About 1 /60	About 1/W
H	L	L	About 1/1 00	About 1 /120
H	L	H	About 1/2 000	
L	H	H	About 1/5. 000	
H	H	H	About 1/12 000	

3. EE Control mode

SMD1 **(Pin 58)= High level**

EEUD	EENR	
	L	Shutter speed up
H		
		Control stopped
	H	
L		Shutter speed down

- When EENR and EEUD are H level, control is stopped.
- When either EENR or EEUD is L level, control is resumed
- The shutter speeds changes in the table below.

SMD2 (Pin 59)	SMD3 (Pin 60)	SMD4 (Pin 61)	SHUTTER SPEED (s)
H	1 -	1 - 1	Max. shutter spaad : 1/100 000 s
L	1 -	1 - 1	Max. shutter spaad : 1/39 000 s
–	H	–	Start shutter speed : 1/1 00 000 s
–	L	–	Start shutter spaed : 1/2000 s

Shutter speed changes at Electronic Exposure Control mode.

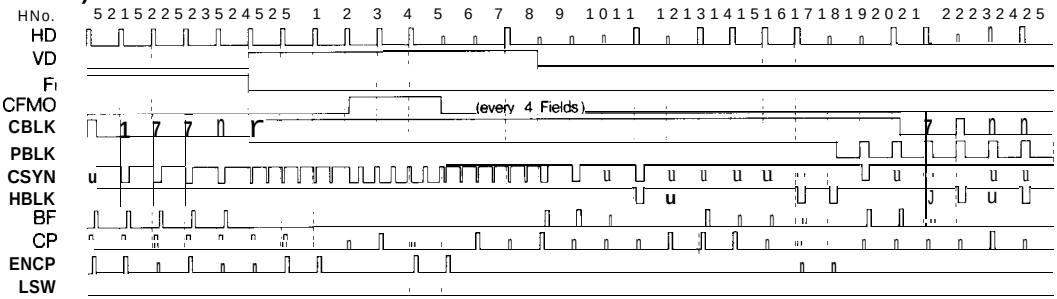
NTSC			PAL		
NO.	CHARGE TIME	SHUTTER SPEED	NO.	CHARGE TIME	SHUTTER SPEED
1	252 H+ α	1 /62 s	1	302 H+ β	1 /52 s
	(by 10 H step)			(by 10 H step)	
19	72 H+ α	1/217 s	24	72 H+ β	1/216 s
	(by 4 H step)			(by 4 H step)	
30	28 H+ α	1 /555 s	35	28 H+ β	1/551 s
	(by 2 H step)			(by 2 H step)	
37	14 H+ α	1/1096s	42	14 H+ β	1/1069s
	(by 1 H step)			(by 1 H step)	
44	7 H+ α	1/2138 s	49	7 H+ β	1/2125 s
	1(by 0.5 H step)			(by 0.5 H step)	
50	4 H+ α	1/3 609 s	55	4 H+ β	1/3 590 s
	(by 0.25 H step)			(by 0.25 H step)	
62	1 H+ α	1/12287 S	67	1 H+ β	1/12254 S
	(by 0.125 H step)			(by 0.125 H step)	
70	0.280 H	1/56 088 s	75	0.275 H	1/% 801 S
71	0.155 H	1/101 436 S	76	0.152 H	1 /102 726 S

α =0.360 H β =0.353 H

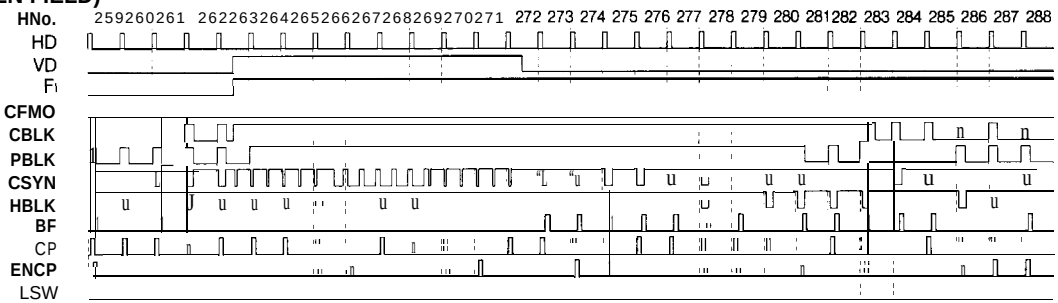
TIMING DIAGRAM

SYNCHRONIZING VERTICAL PULSE < NTSC >

(ODD FIELD)

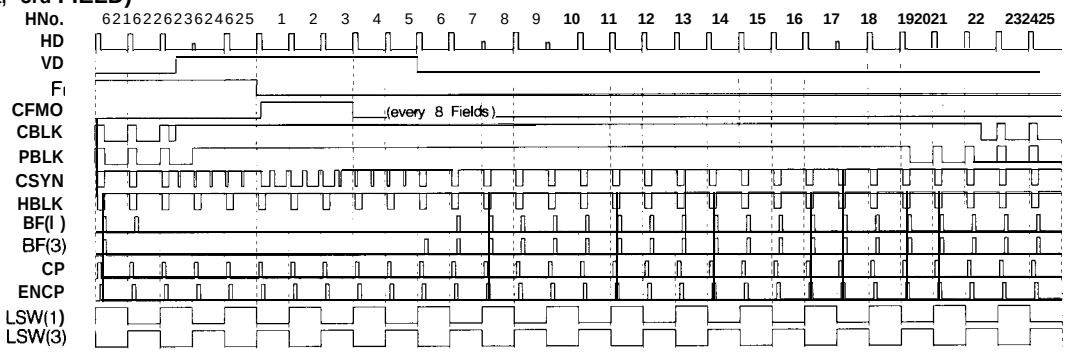


(EVEN FIELD)

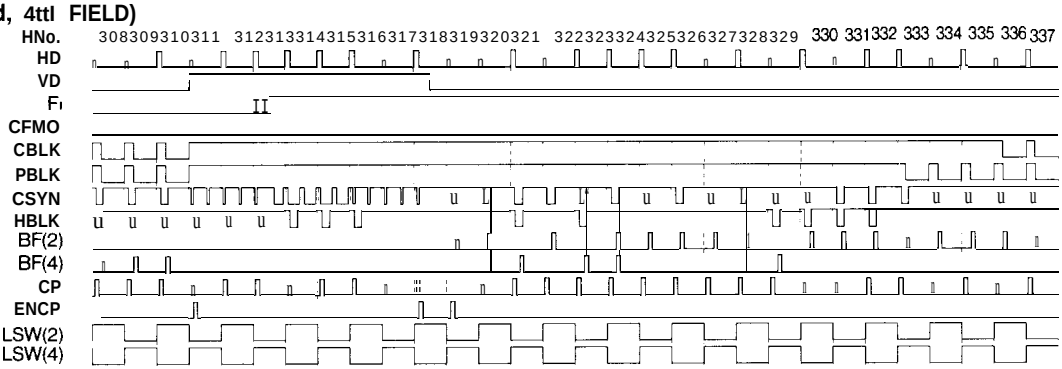


SYNCHRONIZING VERTICAL PULSE < PAL >

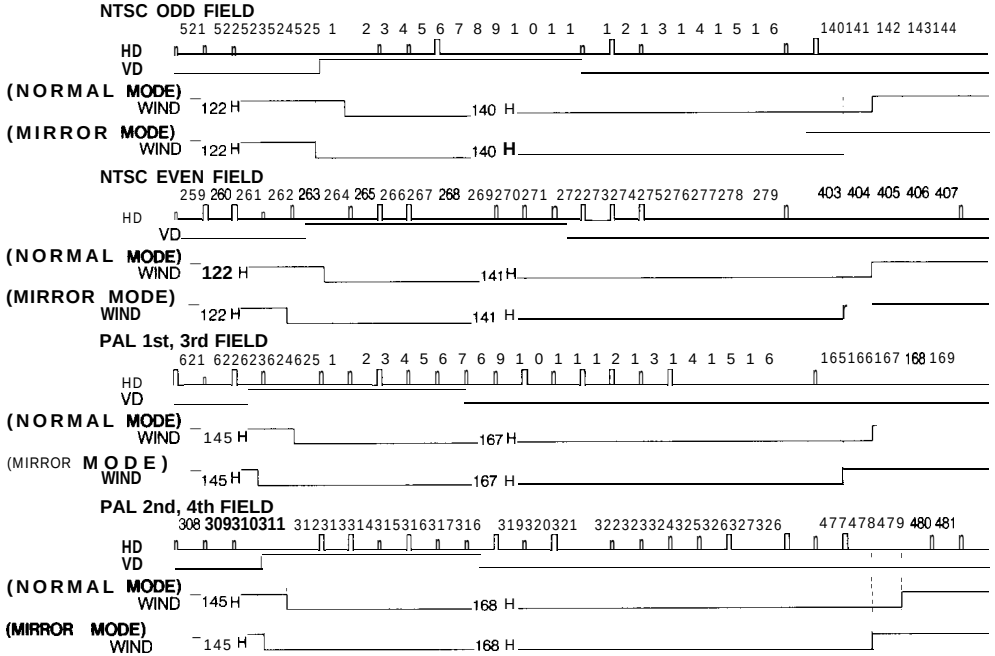
(1St, 3rd FIELD)



(2nd, 4ttl FIELD)

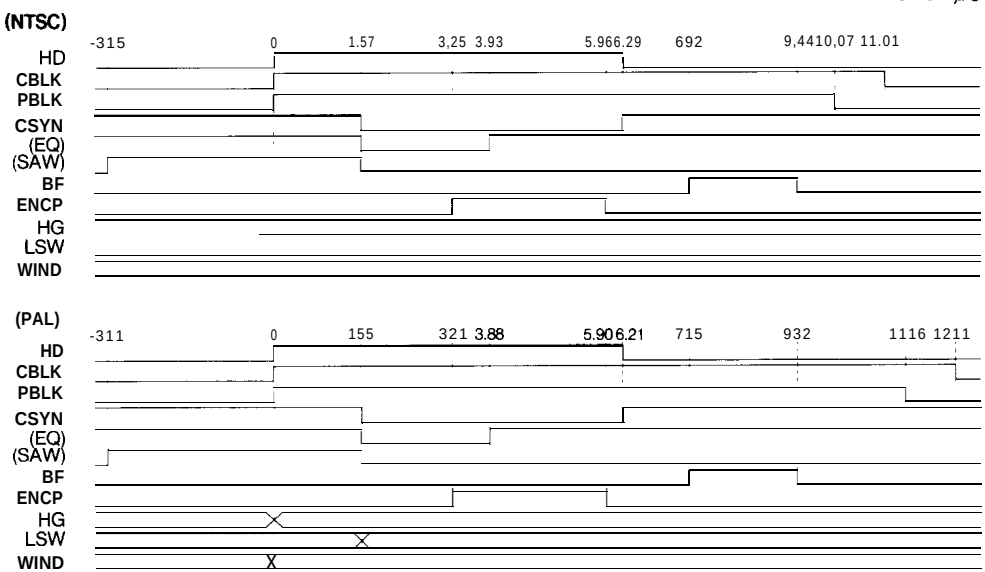


SYNCHRONIZING VERTICAL PULSE

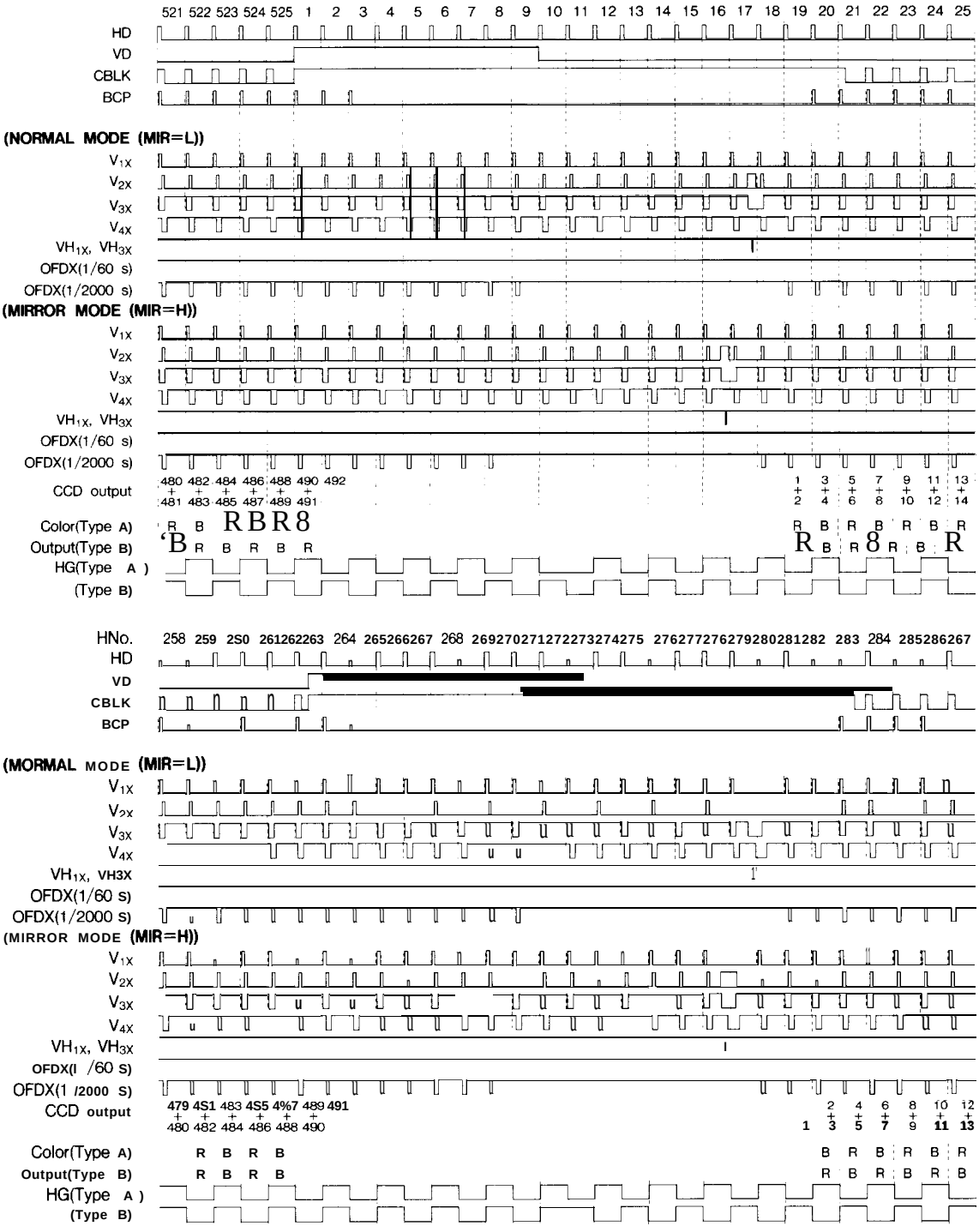


SYNCHRONIZING HORIZONTAL PULSE < NTSC >

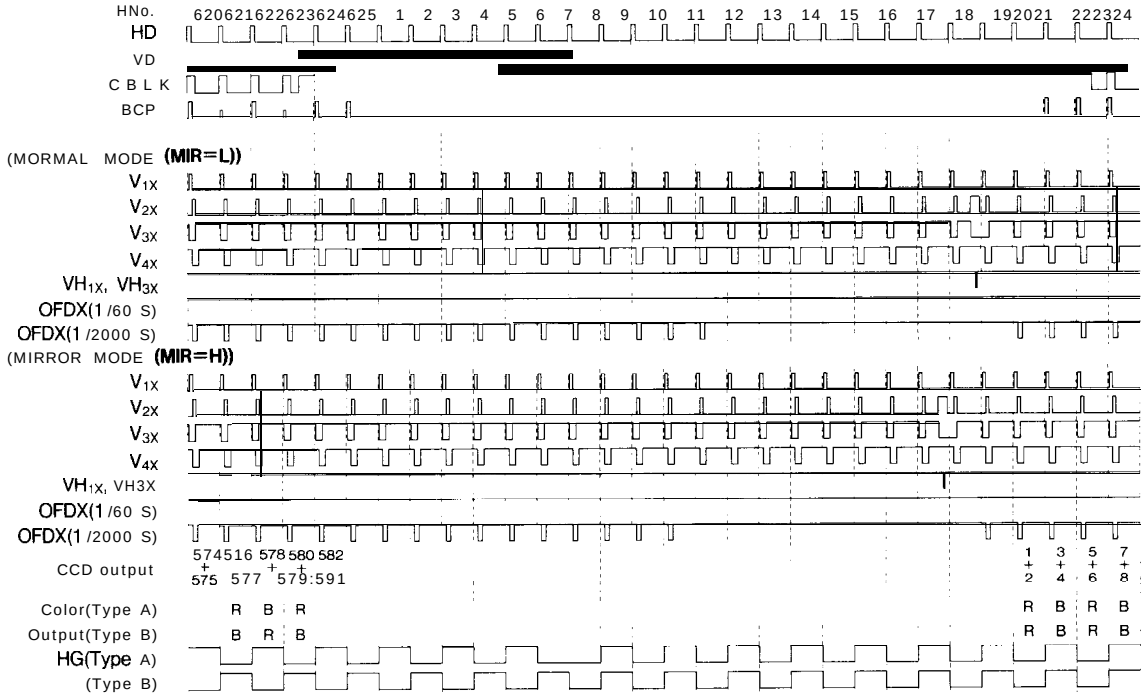
Unit : μs

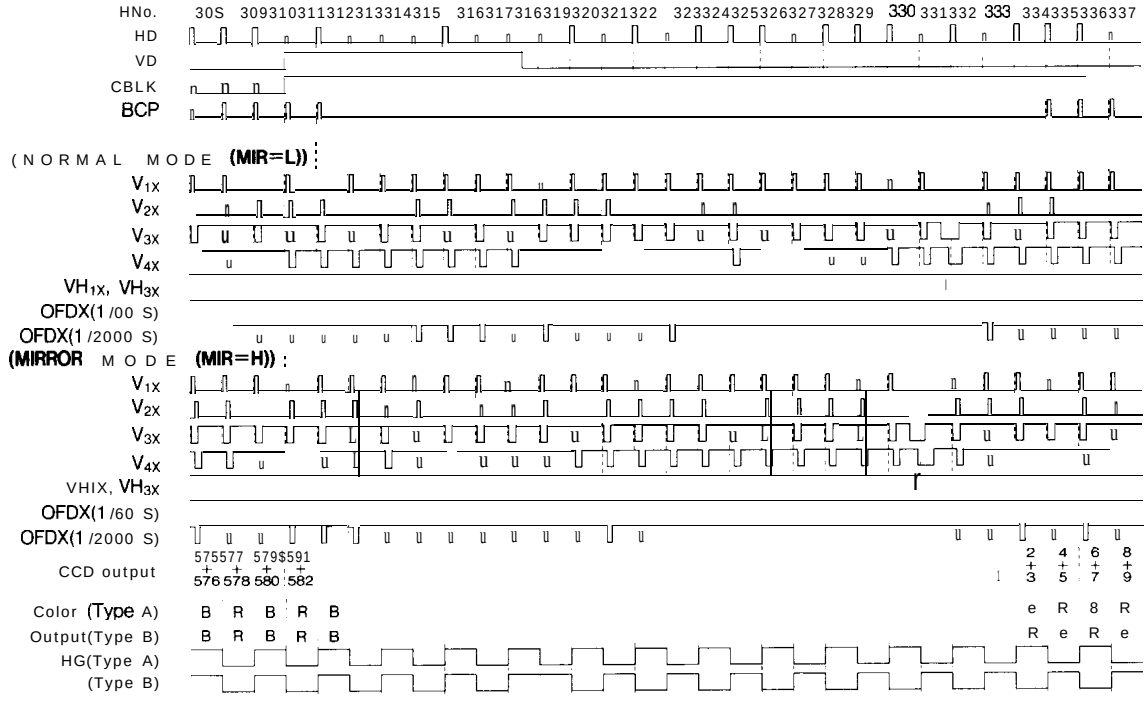


VERTICAL PULSE FOR DRIVING CCD< NTSC >



VERTICAL PULSE FOR DRIVING CCD < PAL >

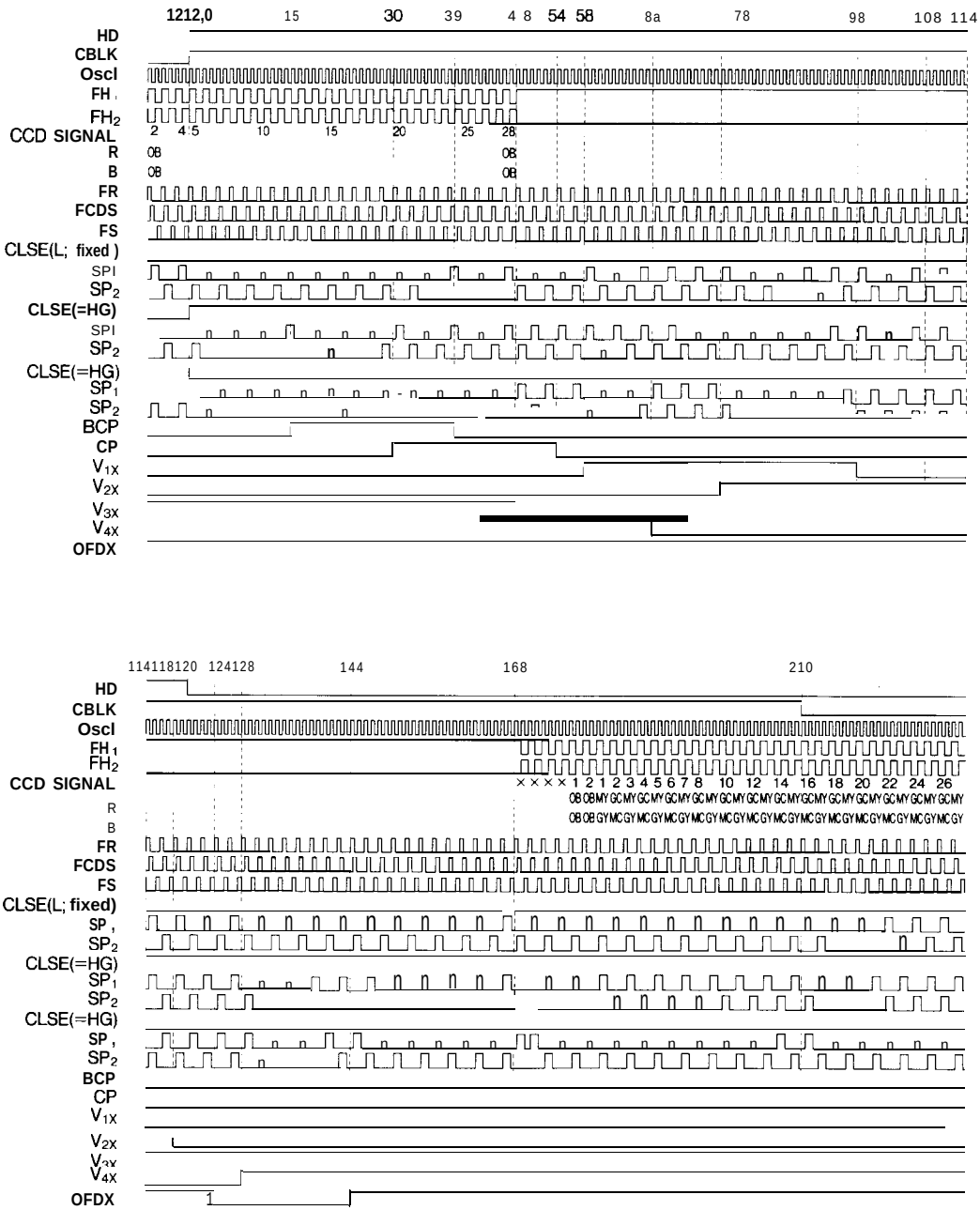




HORIZONTAL PULSE FOR DRIVING CCD < NTSC >

< TYPE-A, NORMAL MODE >

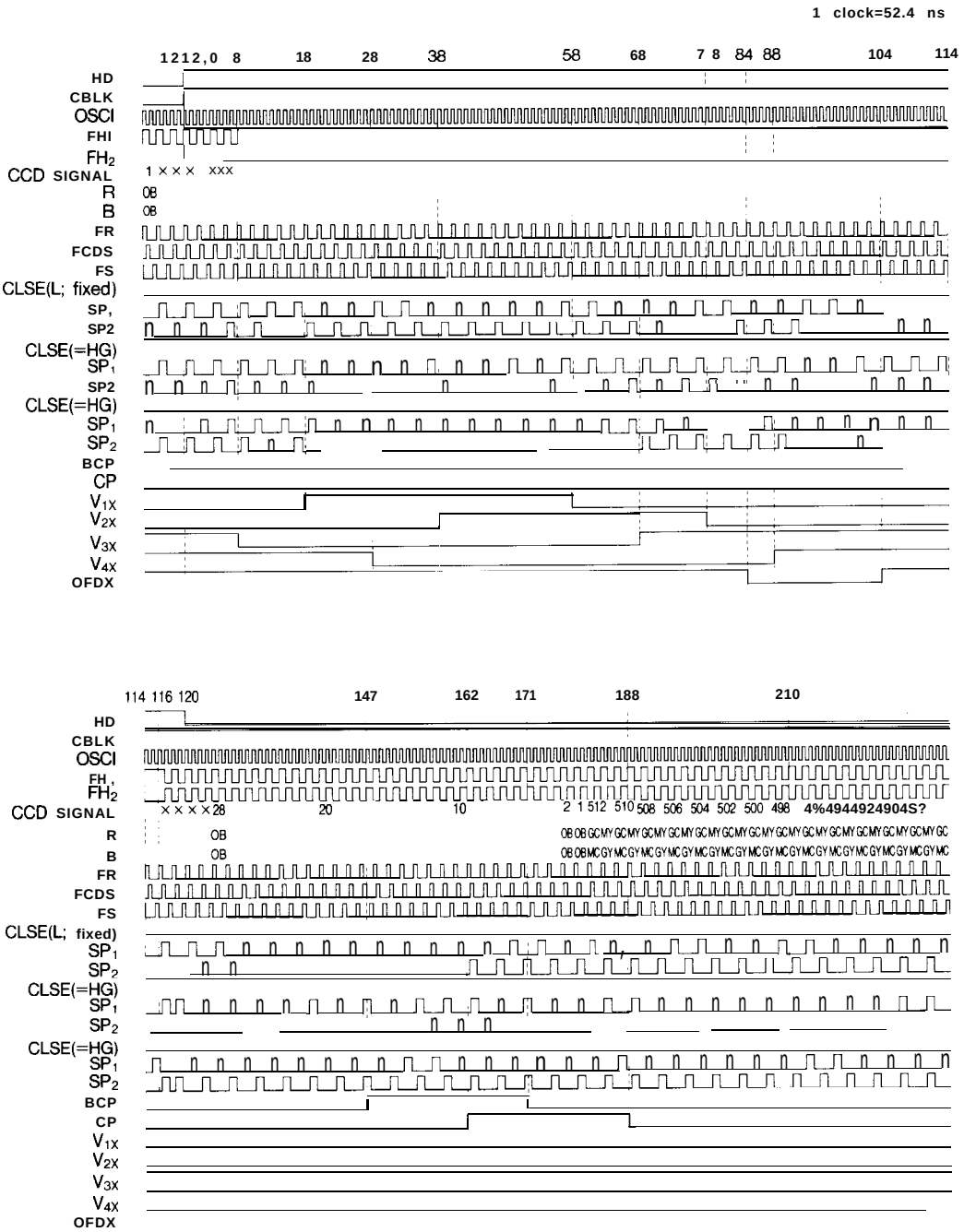
1 clock=52.4 ns



* At SESL=L : When SESL=H, SP_1 and SP_2 is delayed about 52 ns.

HORIZONTAL PULSE FOR DRIVING CCD < NTSC >

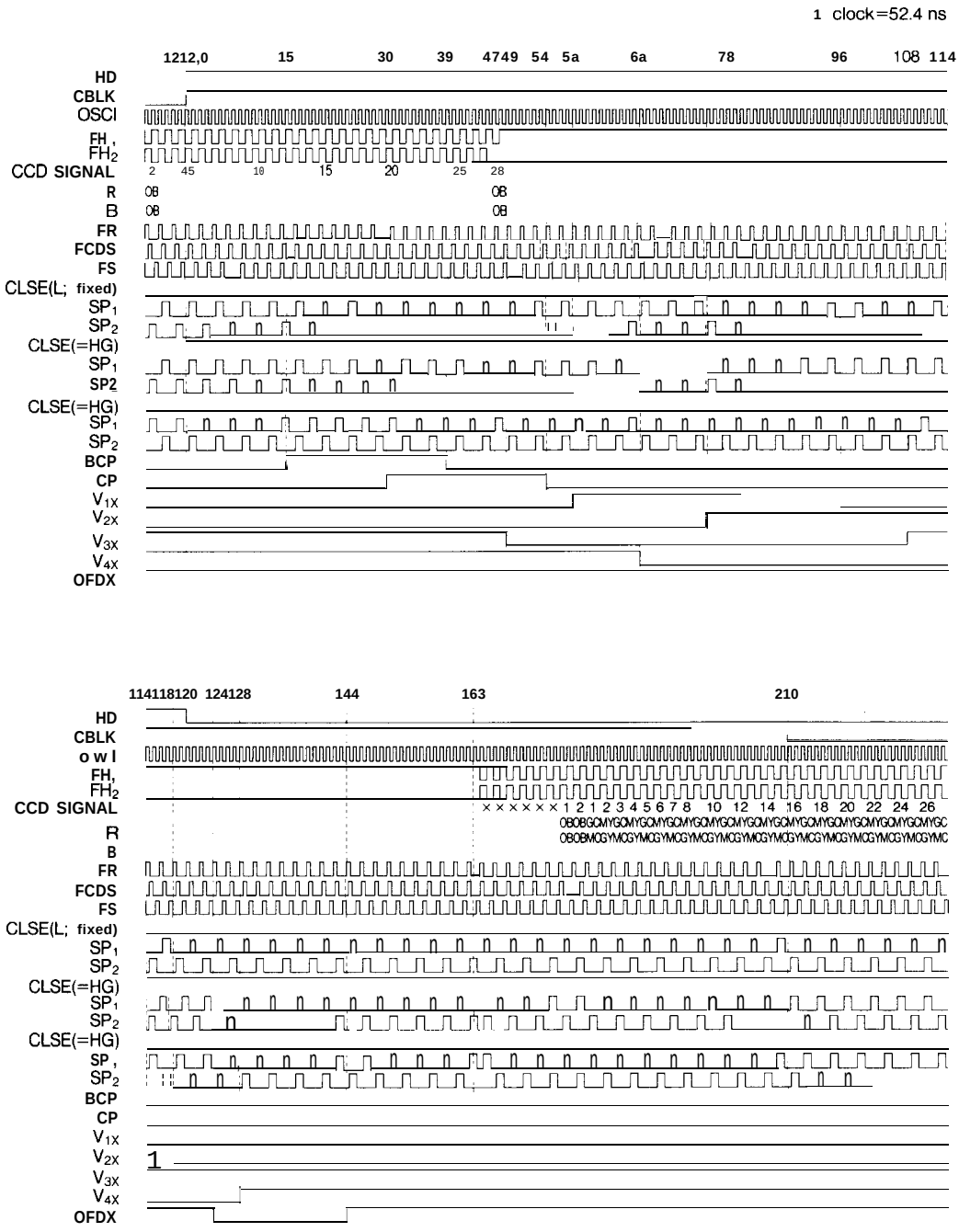
< TYPE-A, MIRROR MODE >



* At SESL=L : When SESL=H, SP_1 and SP_2 is delayed about 52 ns.

HORIZONTAL PULSE FOR DRIVING CCD < NTSC >

< TYPE-B, NOMAL MODE >

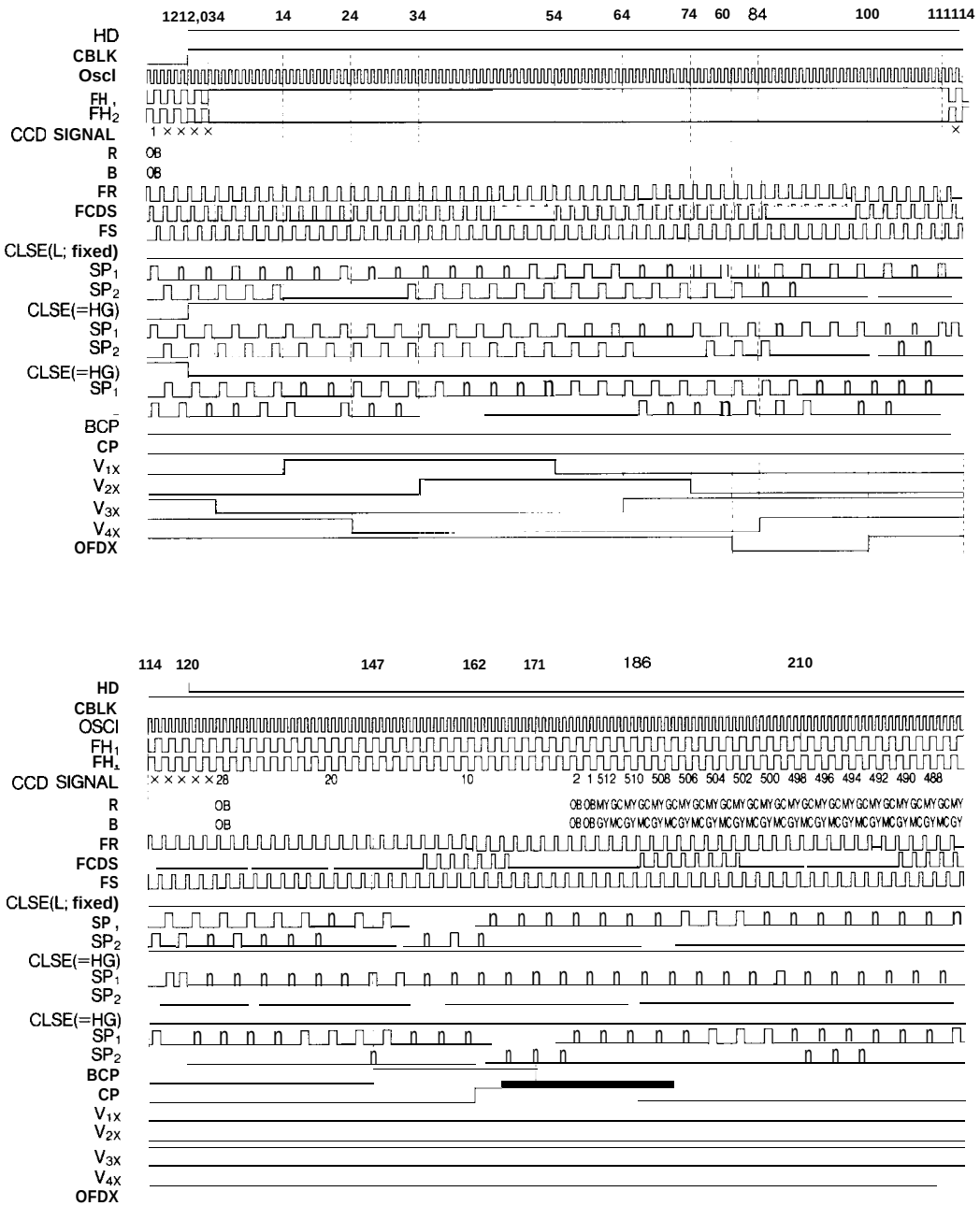


∗At SESL=L : When SESL=H, SPI and SP_2 is delayed about 52 ns

HORIZONTAL PULSE FOR DRIVING CCD < NTSC >

< TYPE-B, MIRROR MODE >

1 clock=52.4 ns

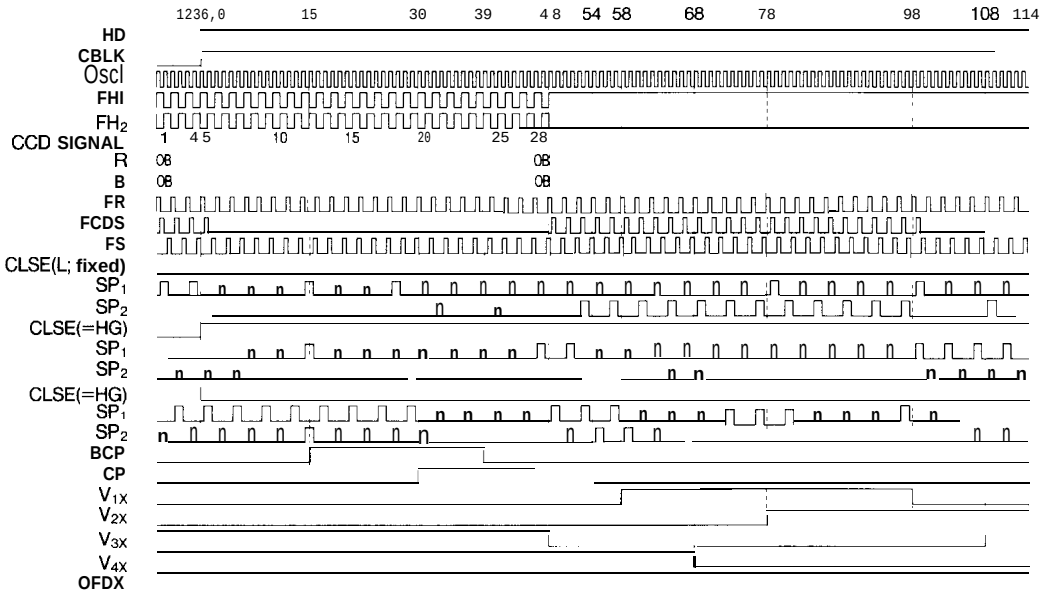


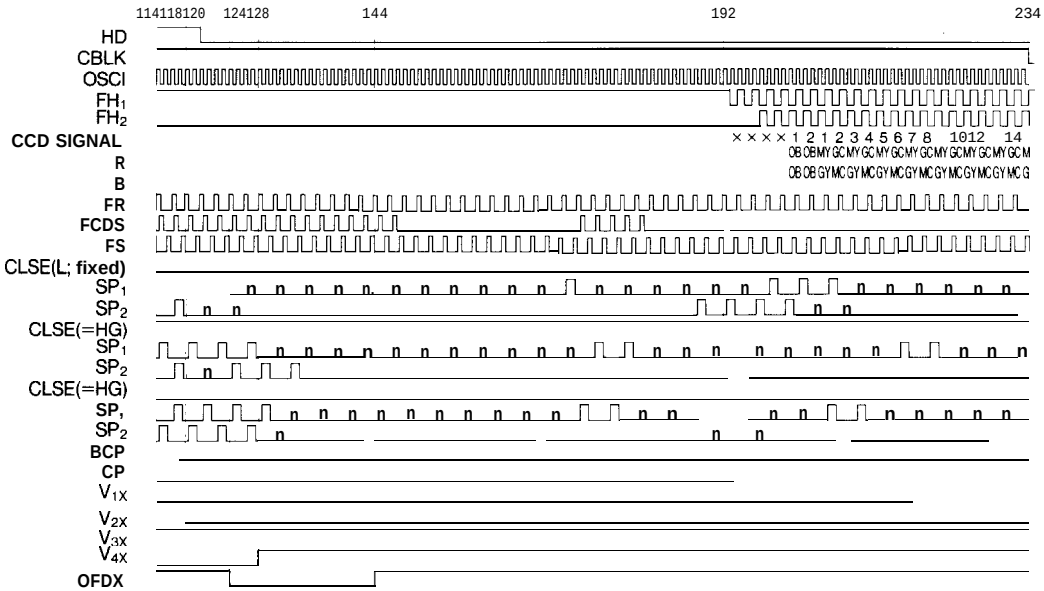
∗ At SESL=L : When SESL=H, SP_1 and SP_2 is delayed about 52 ns.

HORIZONTAL PULSE FOR DRIVING CCD < PAL >

< TYPE-A, NORMAL MODE >

1 clock =51.8 ns

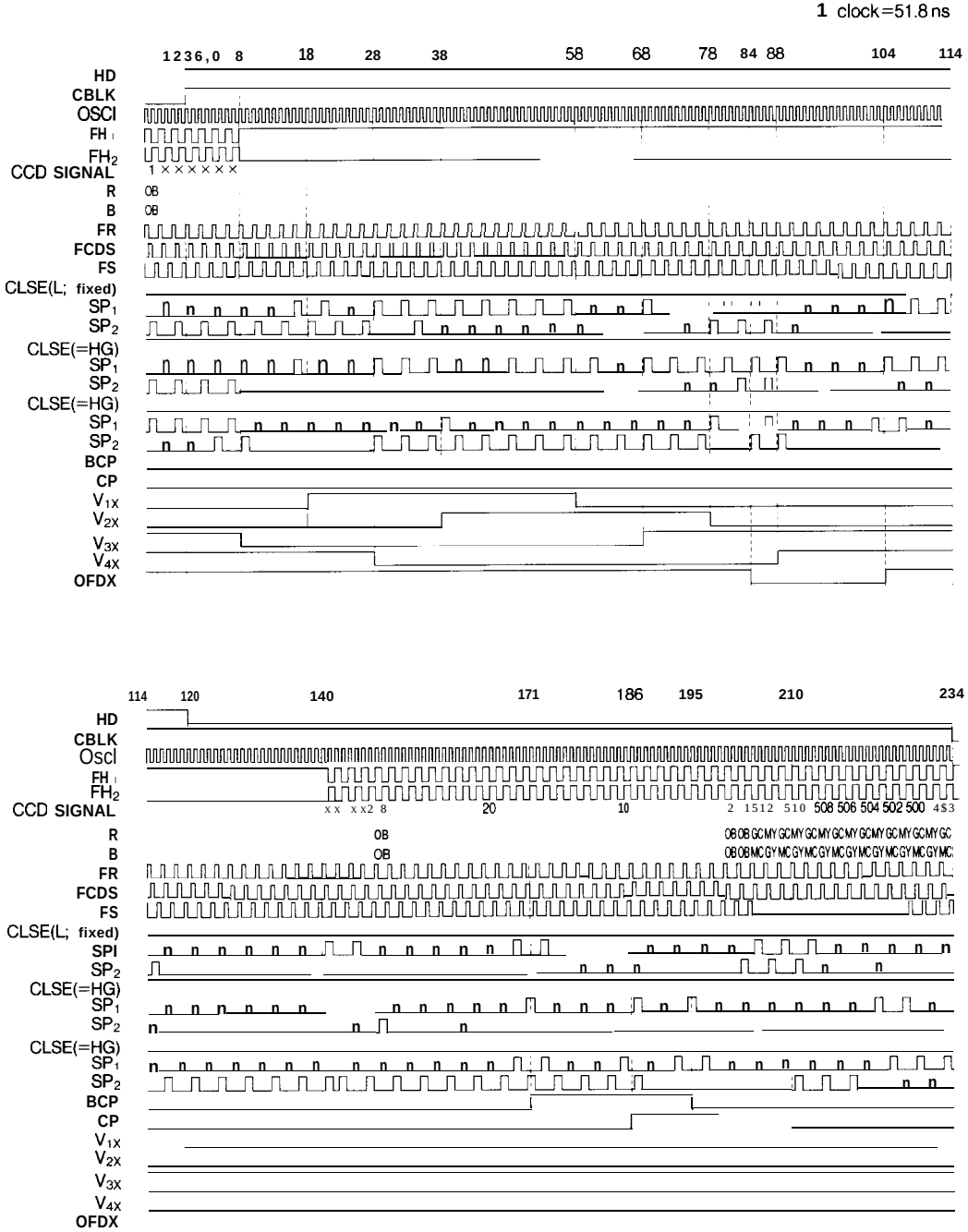




∗ **At SESL=L : When SESL=H, SPI and SP_2 is delayed about 52 ns.**

HORIZONTAL PULSE FOR DRIVING CCD < PAL >

< TYPE-A, MIRROR MODE >

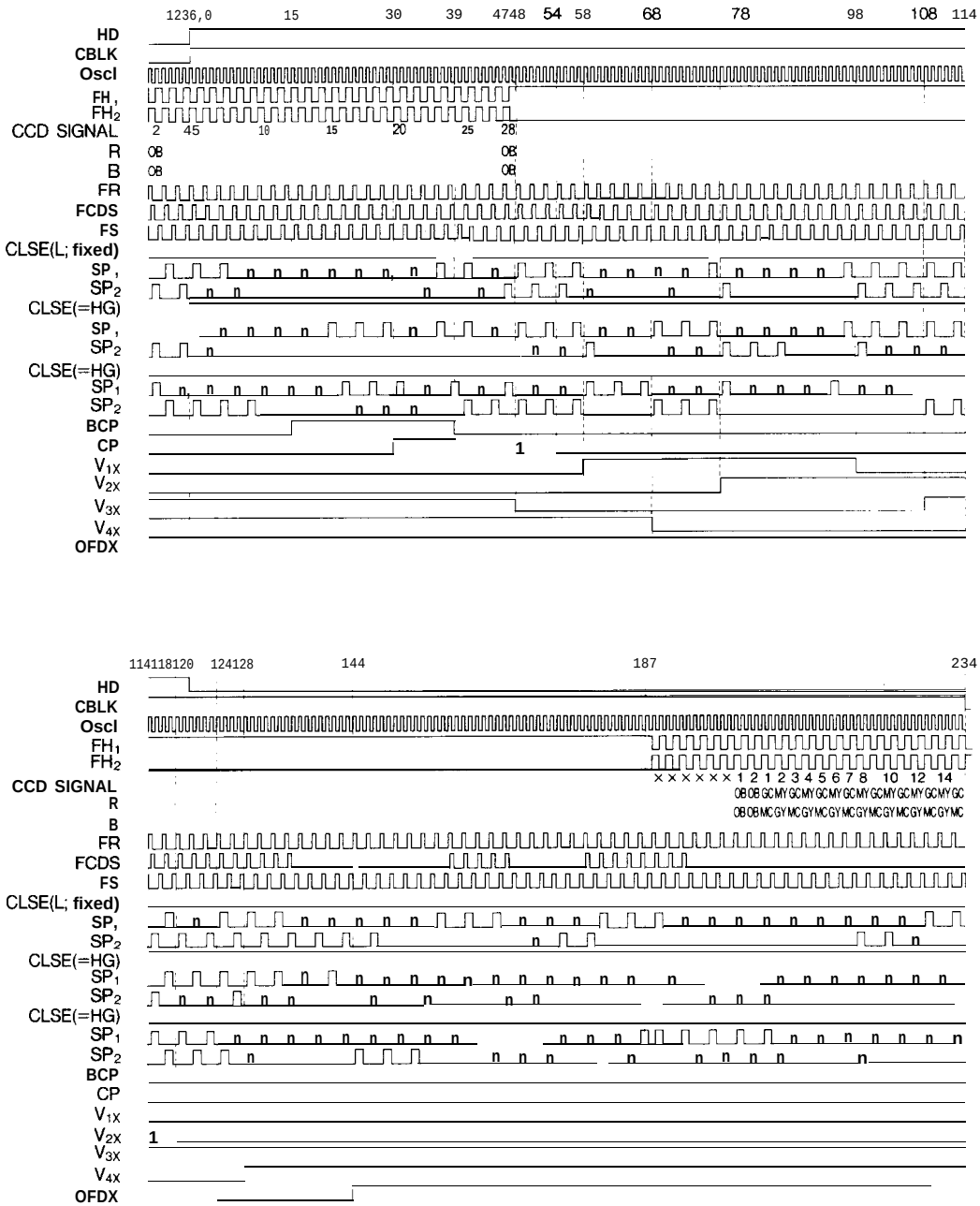


* At **SESL=L** : When SESL=H, SPI and SP_2 is delayed about 52 ns.

HORIZONTAL PULSE FOR DRIVING CCD < PAL >

< TYPE-B, NORMAL MODE >

1 clock=51.8 ns

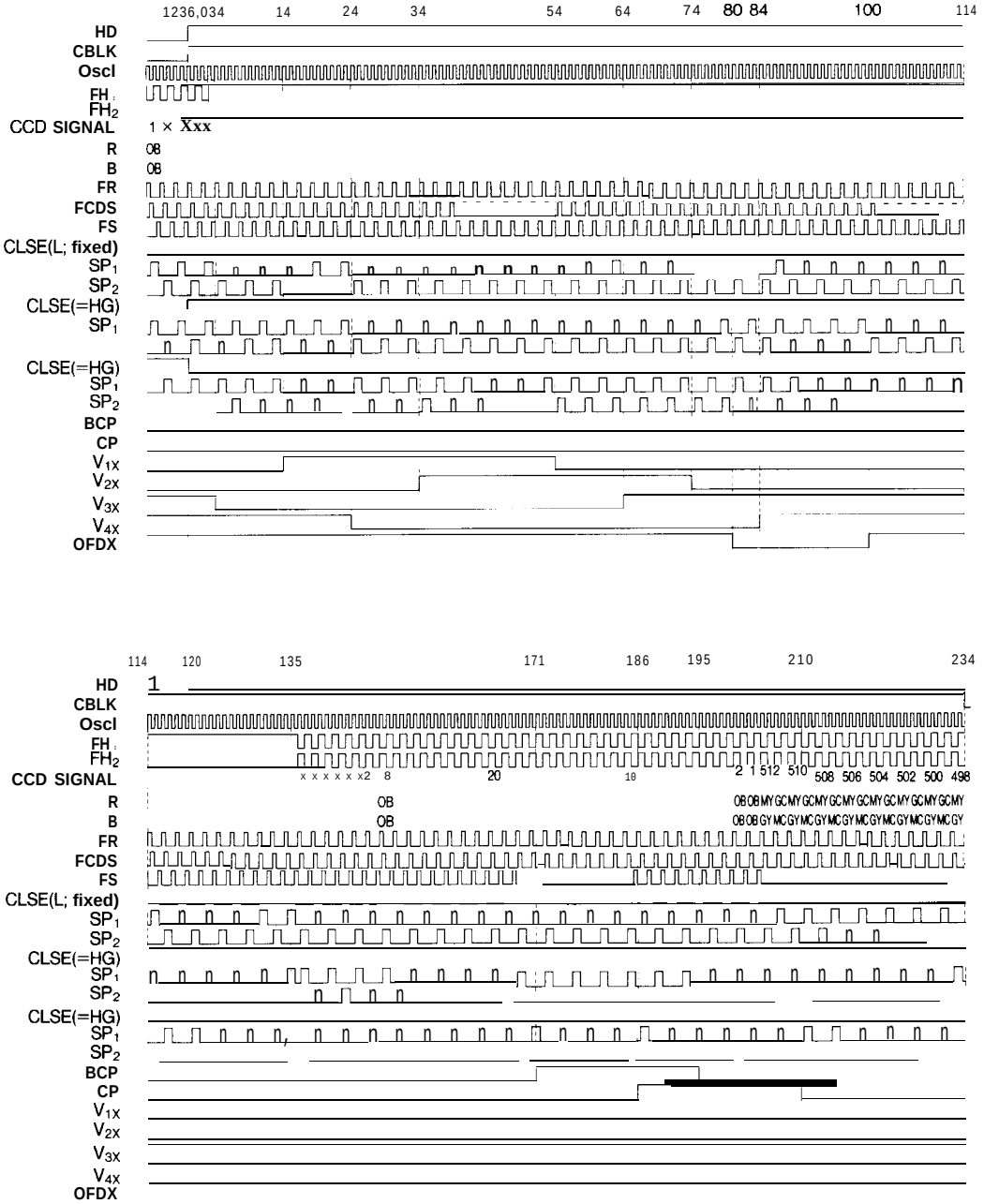


∗ At SESL=L : When SESL=H, SPI and SP_2 is delayed about 52 ns.

HORIZONTAL PULSE FOR DRIVING CCD < PAL >

< TYPE-B, MIRROR MODE >

1 clock =51.8ns

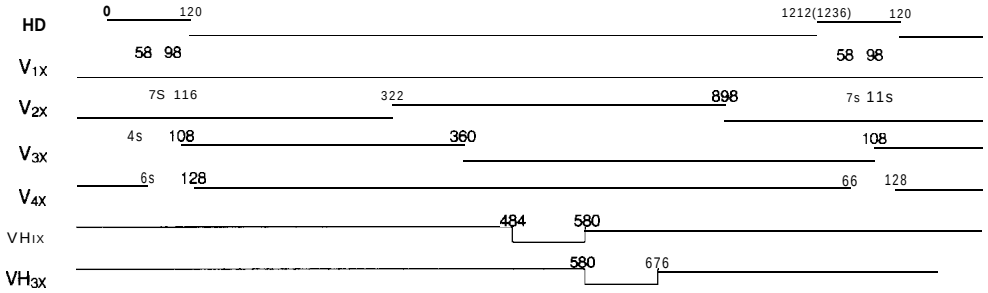


∗ At SESL=L : When SESL=H, SPI and SP_2 is delayed about 52 ns.

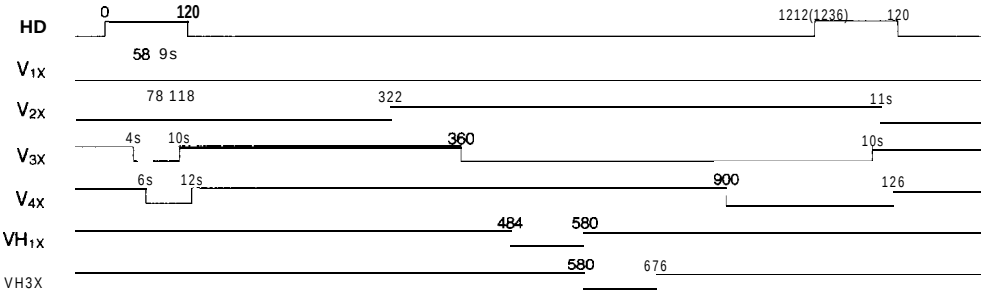
READ OUT PULSE < TYPE-A AND -B, NORMAL MODE >

The number : OSCI clock pulse, 1 clock=52.4 ns (51.8 ns), ( ) : PAL

(ODD (1st, 3rd) FIELD)



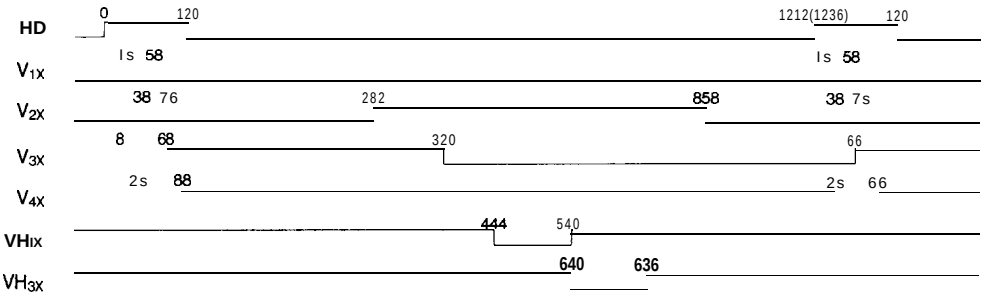
(EVEN (2nd, 4th) FIELD)



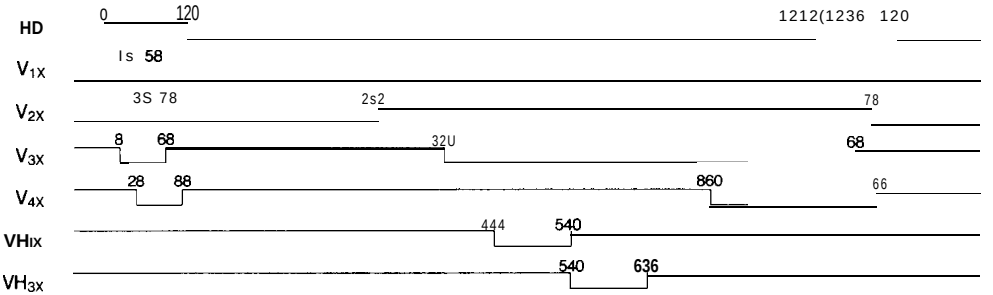
READ OUT PULSE < TYPE-A, MIRROR MODE >

The number : OSCI clock pulse, 1 clock=52.4 ns (51.8 ns), ( ) : PAL

(ODD (1st, 3rd) FIELD)



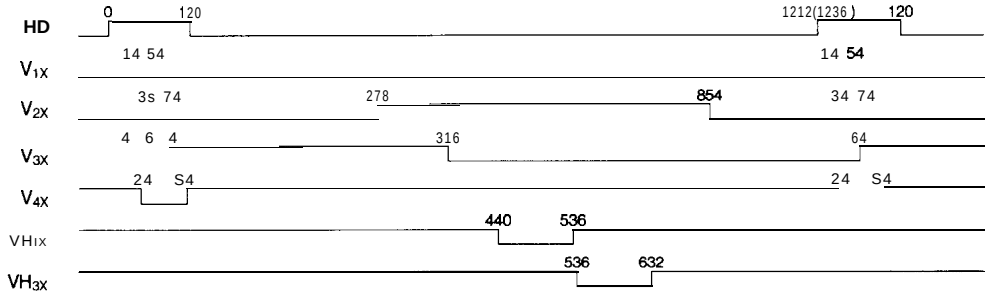
(EVEN (2nd, 4th) FIELD)



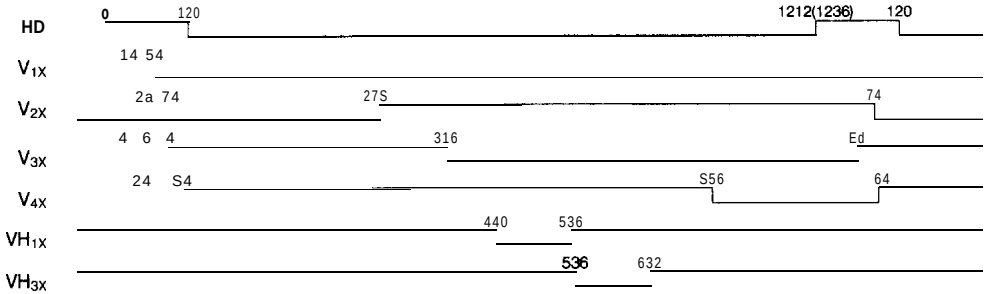
READ OUT PULSE < TYPE-B, MIRROR MODE >

The number : OSCI clock pulse, 1 clock=52.4 ns (51.8 ns), ( ) : PAL

(ODD (1st, 3rd) FIELD)

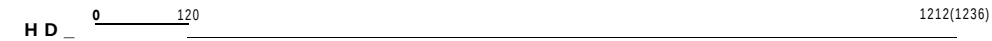


(EVEN (2nd, 4th) FIELD)

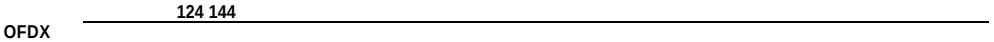


SHUTTER PULSE < TYPE-A AND -B, NORMAL MODE >

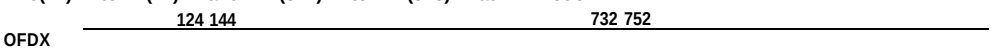
The number : OSCI clock pulse, 1 clock=52.4 ns (51.8 ns), ( ) : PAL



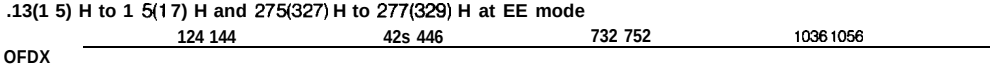
. Fixed Shutter mode and E/E Control mcrde except 10(12) H to 18(20) H and 272(324) H to 280(332) H



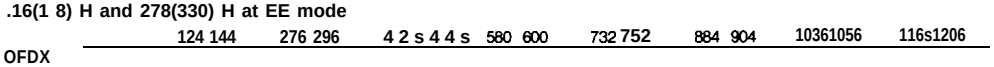
. 10(12) H to 12(14) H and 272(324) H to 274(328) H at EE mode



.13(1 5) H to 1 5(17) H and 275(327) H to 277(329) H at EE mode



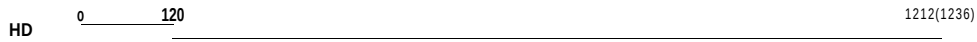
.16(1 8) H and 278(330) H at EE mode



. 17(19) H and 279(331) H at EE mode

SHUTTER PULSE < TYPE-A, MIRROR MODE >

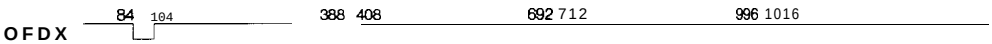
The number : OSCI clock pulse, 1 clock =52.4 ns (51.8 ns), ( ) : PAL



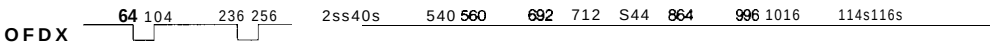
. Fixed Shutter mode and E/E Control mode except 9(11) H to 17(19) H and 271(323) H to 279(331) H

•9(1 1) H to 11(13) H and 271(323) H to 273(325) H at EE mode

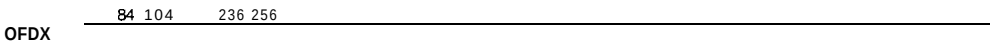
.12(1 4) H to 1416) H and 274(326) H to 276(328) H at EE mode



. 15(1 7) H and 277(329) H at EE mode

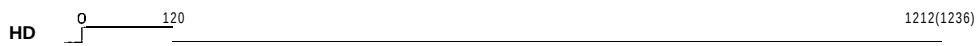


• 16(18) H and 276(330) H at EE mode

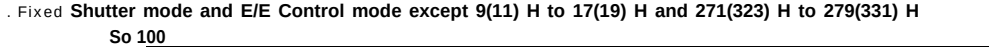


SHUTTER PULSE < TYPE-B, MIRROR MODE >

The number : OSCI clock pulse, 1 clock =52.4 ns (51.8 ns), ( ) : PAL

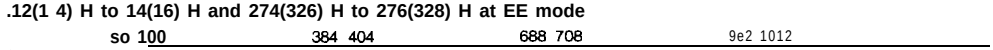


. Fixed **Shutter mode and E/E Control mode except 9(11) H to 17(19) H and 271(323) H to 279(331) H**

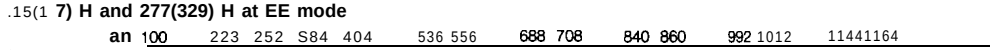


•9(1 1) H to 11(13) H and 271(323) H to 273(325) H at EE **mode**

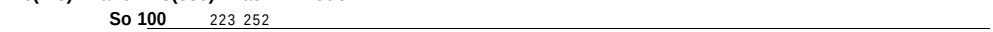
.12(1 4) H to 14(16) H and 274(326) H to 276(328) H at EE mode



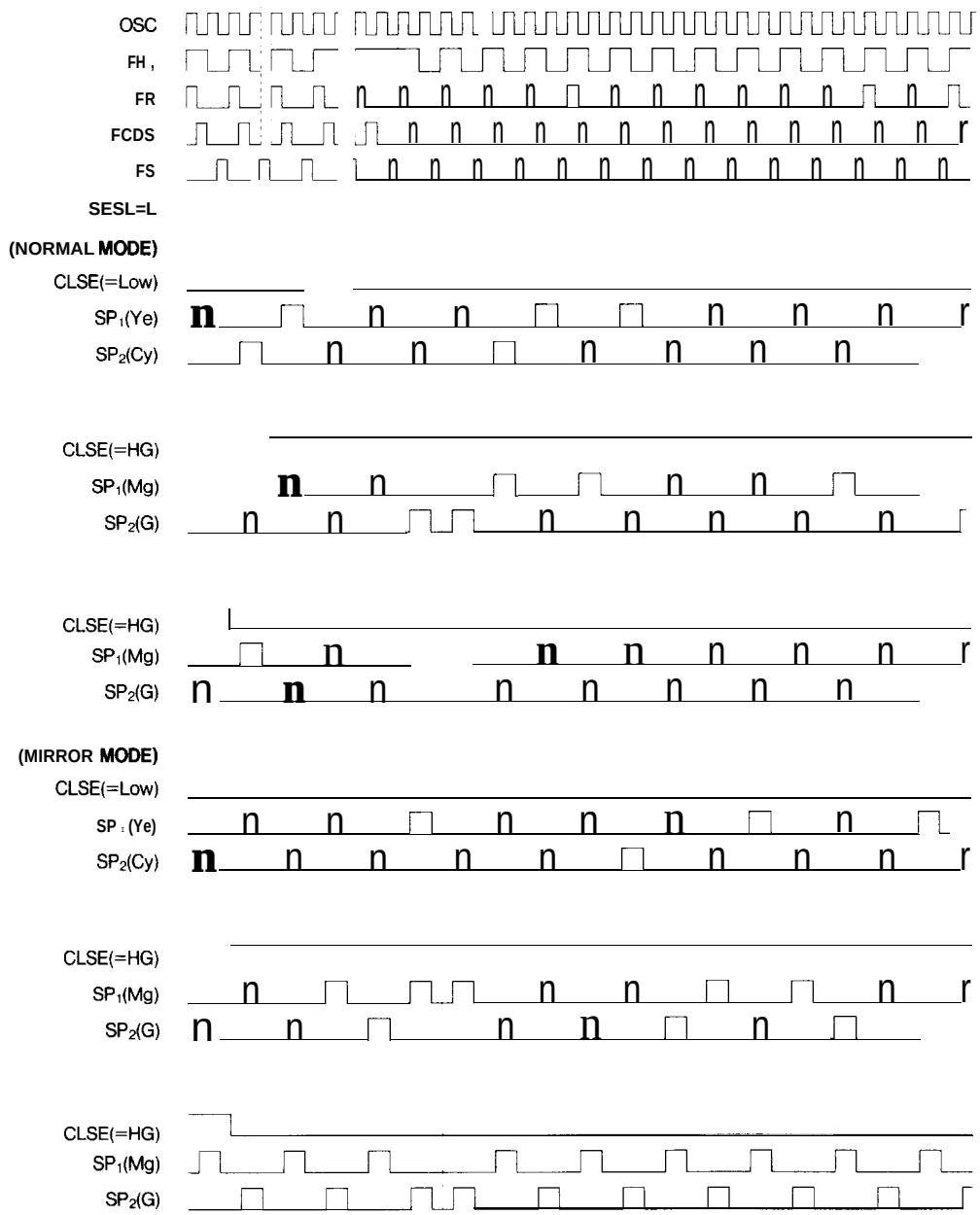
.15(1 **7) H and 277(329) H at EE mode**



.16(1 8) H and 278(330) H at EE mode

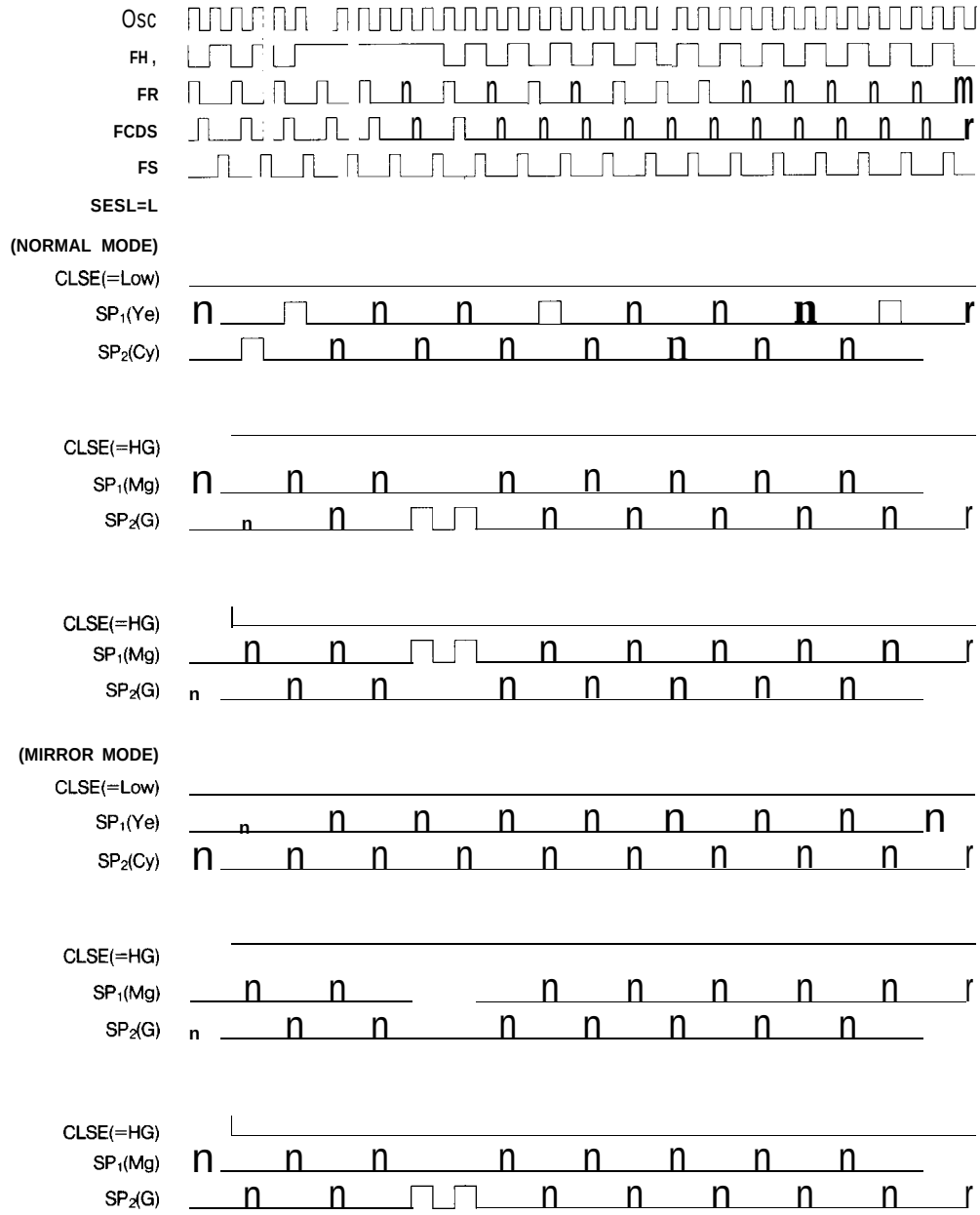


COLOR SEPARETE PULSE < TYPE-A (SLCT=L) >



The SP_1 and SP_2 pulse is delayed about 52 ns at SESL=H.

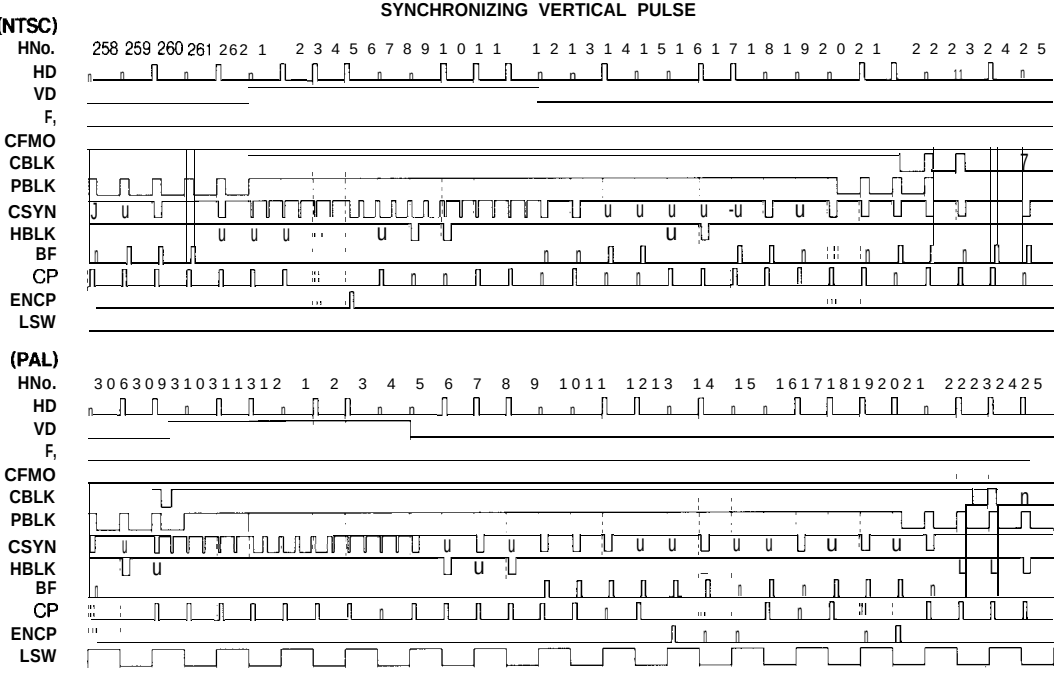
COLC SEPARATE PULSE < TYPE-B (SLCT=H)>



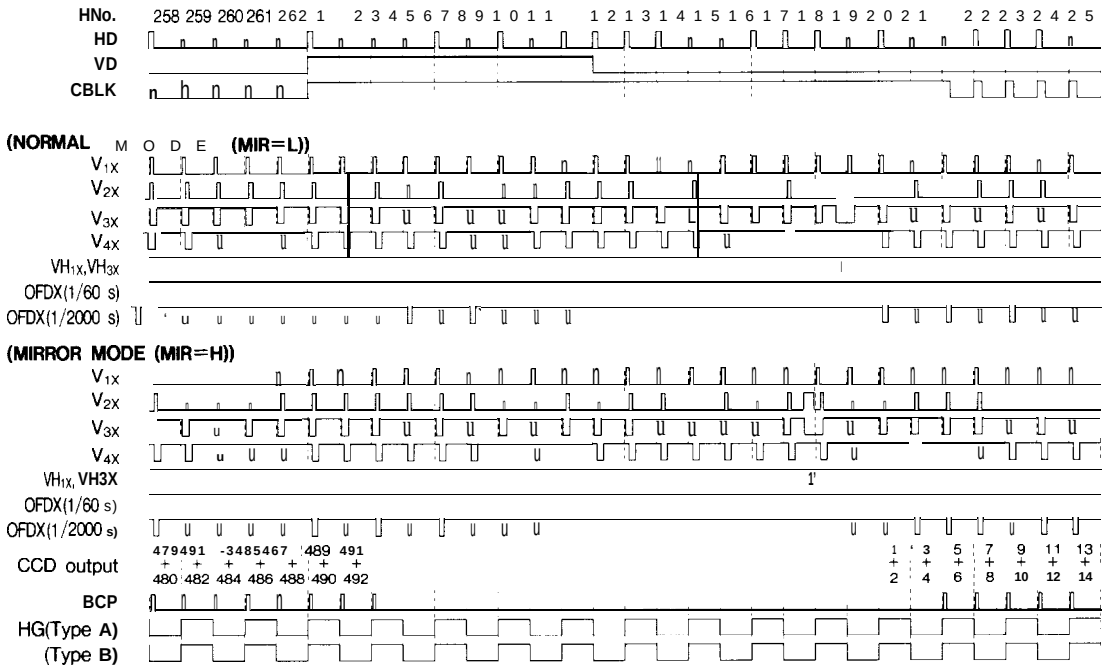
The SP_1 and SP_2 pulse is delayed about 52 ns at SESL=H

NON-INTERLACE MODE

SYNCHRONIZING VERTICAL PULSE



VERTICAL PULSE FOR DRIVING CCD < NTSC >



NON-INTERLACE MODE

VERTICAL PULSE FOR DRIVING CCD < PAL >